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REMARKS

SUMMARY OF INTERVIEW

Applicant wishes to thank Examiner Ko for the interview conducted on July 13, 2006. The following summarizes the substance of the interview, in accordance with the guidelines provided by MPEP 713.04.

(A) No exhibit was shown, and no demonstration was conducted.

(B) Claim 21 was discussed.

(C) The teachings of Grimsrud *et al.* (U.S. Patent No. 7,000,077) were primarily discussed.

(D) No proposed amendments were discussed.

(E) The general thrust of Applicant's arguments presented at the interview was that Grimsrud does not teach or suggest the cache demand circuit as claimed. The Examiner indicated that a response summarizing these arguments should be presented.

The Applicant thanks the Examiner for his careful and thoughtful examination of the present application and for the interview granted on July 13, 2006. By way of summary, Claims 21-44 were pending in this application. In this response, the Applicant has made no amendments. Accordingly, Claims 21-44 remain pending for consideration.

REJECTION OF CLAIMS 21-24, 28-30, 34-37 AND 40-42 UNDER 35 U.S.C. § 102(e)

The Office action rejected Claims 21-24, 28-30, 34-37 and 40-42 under § 102 as being anticipated by U.S. patent no. 7,000,077, issued to Grimsrud *et al.* (Grimsrud). Applicant respectfully submits that Grimsrud fails to identically teach every element of these claims. *See* M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

For example, Claim 21 recites: a cache demand circuit for receiving an address from the micro-controller and transmitting the address to a micro-controller cache system, wherein the micro-controller cache system is responsive to the transmitted address to fetch micro-controller executable data **stored at the transmitted address** before a micro-controller requests execution of the micro-controller executable data. (Emphasis added.) Grimsrud neither teaches nor discloses these limitations.

First, the Examiner calls out micro-controller 40, in Figure 3, as corresponding to the micro-controller of Claim 21, and calls out the storage cache 50 as corresponding to the micro-controller cache system. Applicant respectfully submits that the micro-controller 40 does not correspond to the micro-controller in Claim 21. Grimsrud's micro-controller 40 does not "request execution of micro-controller executable data" stored at an address transmitted to the storage cache 50, as required by Claim 21. Instead, Grimsrud teaches a storage system that uses prefetch algorithms to prefetch data from a disk to the storage cache 50 so that the prefetched data can be more efficiently returned to the host. Col. 4, ll. 41-67. Thus, the prefetched data fetched by the storage cache 50 is simply forwarded to the host, and the micro-controller 40 does not request execution of this data. For at least this reason, Grimsrud does not disclose that the micro-controller cache system fetches micro-controller executable data before the micro-controller requests execution of the micro-controller executable data.

Second, as discussed during the Applicant's recent interview, the Examiner cites the prefetch algorithms 112 of Grimsrud as corresponding to the cache demand circuit of Claim 21. As described in Grimsrud, a host driver "tells the storage system which demand blocks to read, and gives the storage system the address of the driver's buffer memory. The storage system decides which blocks to prefetch and return with the demand blocks, according to the prefetch algorithms." Col. 6, ll. 20-25. Thus, the prefetch algorithms 112 taught by Grimsrud use the well-known caching methodology of receiving an address from a micro-controller, and then using that address to prefetch data at one or more prefetch addresses derived from the received address, as discussed in the background of Applicant's specification (p. 1, ll. 22-24). These prefetch algorithms 112 are not used to prefetch data stored at the received address (because

the received address is associated with a micro-controller request). In contrast, the claimed cache demand circuit receives an address from the micro-controller, transmits that same address to the cache system, and the cache system prefetches data stored at that same transmitted address before the micro-controller requests execution of the data at that address. The disclosure in Grimsrud simply does not teach such a structure.

For at least these reasons, Claim 21 should not be rejected as anticipated by Grimsrud.

Claim 34 recites: receiving at the cache demand circuit an address in the remote memory from the micro-controller, transmitting the address from the cache demand circuit to the micro-controller cache system, and caching the micro-controller executable data **stored at the address** before the micro-controller requests execution of the micro-controller executable data. Grimsrud neither teaches nor discloses this limitation.

For reasons similar to those discussed above with respect to Claim 21, Applicant submits that Grimsrud neither teaches nor discloses these limitations.

For at least these reasons, Claim 34 should not be rejected as anticipated by Grimsrud.

Claims 22-33, which depend from Claim 21, and Claims 35-44, which depend from Claim 34, are believed to be patentable for at least the same reasons articulated above, and because of the additional features recited therein.

REJECTION OF CLAIMS 25-27, 31-33, 38-39 AND 43-44 UNDER 35 U.S.C. § 103(a)

The Office action rejected Claims 25-27, 31-33, 38-39 and 43-44 under 35 U.S.C. § 103 as being unpatentable over Grimsrud in view of U.S. patent no. 6,789,132, issued to Hoskins (Hoskins).

REFERENCES FAIL TO TEACH ALL OF THE CLAIMED ELEMENTS

Applicant respectfully submits that Grimsrud, alone or in combination with Hoskins, fails to teach or suggest all of the elements of the rejected claims. *See* M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations).

The limitations discussed above with reference to Claims 21 and 34 are not taught or suggested by Hoskins. For at least these reasons, Claims 21 and 34 should not be rejected as obvious over Grimsrud and Hoskins.

Therefore, Claims 25-27 and 31-33, which depend from Claim 21, and Claims 38-39 and 43-44, which depend from Claim 34, are believed to be patentable for at least the same reasons articulated above, and because of the additional features recited therein.

CONCLUSION

In view of the foregoing remarks, Applicant respectfully submits that the pending claims are now in condition for allowance and requests reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: August 30, 2006

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